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10/804,294	03/18/2004	Benjamin J. Esposito	ALTRP092/A1035	7802

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EXAMINER	
YAARY, MICHAEL D	

ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/804,294	ESPOSITO ET AL.	
	Examiner	Art Unit	
	Michael Yaary	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *02/22/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-30 are pending in the application.

Drawings

2. Figure 1A, 1B, 1C, 1D, 3A, and 3B should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 101

3. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

4. As to claims 20 and 30 the claims are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

(i) Claims 29 and 30 are directed to software per se, not tangibly embodied, the computer program product failing to recite any hardware, or a processor to execute the claimed computer code. A suggested way to modify the claims would be in a format such as, "A computer program product, stored on a computer storage media, the computer storage media having computer readable code that when executed by a processor..."

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 2, 5, 7, 9, 11, 18, 20, and 22 are rejected under 35 U.S.C. 112, second paragraph as it unclear if the claims are intended to be independent or dependent claims.

(i) Claim 2 discloses, "A numerically controlled oscillator," which is not consistent with claim 1, which reads, "A multi-channel integrator." Examiner is interpreting claim 2 as dependent on claim 1 for examination purposes.

(ii) Claim 5 discloses in its preamble, "An M channel decimator..." which is not consistent with claim 1, which reads, "A multi-channel integrator..." Examiner is interpreting claim 5 as dependent on claim 1 for examination purposes.

(iii) Claim 7 and 18 disclose "An N stage multi-channel..." which are consistent with claims 1 and 15, which read, "A multi-channel integrator... and a multi-channel differentiator..." Examiner is interpreting claims 7 and 18 as dependent on claims 1 and 15 respectively for examination purposes.

(iv) Claims 9 and 20 disclose "An M channel interpolator..." which are not consistent with claim 1 and 15, which read, "A multi-channel integrator and a multi-channel differentiator..." Examiner is interpreting claims 9 and 20 as dependent on claims 1 and 15 respectively for examination purposes.

(v) Claim 11 and 22, disclose "An N stage multi-channel interpolator..." which are not consistent with claims 1 and 15, which read, "A multi-channel integrator and a multi-channel differentiator..." Examiner is interpreting claims 11 and 22 as dependent on claims 1 and 15 respectively for examination purposes.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1, 15, 29, and 30 are rejected under 35 U.S.C. 102(b) as being anticipated by McCaslin et al. (hereafter McCaslin)(US Pat. 4,999,798).

9. **As to claim 1,** McCaslin discloses a multi-channel integrator (integrator 12 of figure 2) comprising:

An integrator input (input 14 of figure 2);

An integrator output (output of integrator 12 in figure 2);

An adder (adder 44 of figure 2) comprising:

A first adder input connected to the integrator input (input 14 connected to adder 44 in figure 2);

A second adder input (second input of adder 44 in figure 2); and

An adder output (output of adder 44 in figure 2);

A delay section (delay element 46 in figure 2) comprising:

A delay section input (input to delay element 46 in figure 2);

A delay section output (output to delay element 46 in figure 2);

A plurality of delay elements connected in series between the delay section input and the delay section output (delay elements 38, 40, and 42 in series with integrators 38, 40, and 42);

A feedback line connecting the delay section output to the second adder input (delay output feedback to adder 44 in figure 2);

Wherein the adder output is connected to the delay section input (adder output connected to delay element input in delay element 46); and

Further wherein the delay section output is connected to the integrator output (output of figure integrator circuit 12 in figure 2).

10. **As to claim 15,** McCaslin discloses a multi-channel differentiator (differentiator 16 in figure 2) comprising:

A differentiator input (input to differentiator circuit 16 in figure 2);

A differentiator output (output to differentiator circuit 16 in figure 2);

A subtractor (subtractor 68 in figure 2) comprising:

A first subtractor input (subtractor input to subtractor 68);

A second subtractor input (second subtractor input to subtractor 68);

A subtractor output (output of subtractor 68);

A delay section (delay element 70 in figure 2) comprising:

A delay section input connected to the differentiator input (differentiator input connected to delay element 56 input in figure 2);

A delay section output (output of delay element 56);

A plurality of delay elements connected in series between the delay section input and the delay section output (delay elements 56, 58, and 60 connected in series with differentiators 56, 58, and 60);

A feedforward line connecting the differentiator input to the first subtractor input (feedforward line to subtractor 68 in figure 2);

Wherein the delay section output is connected to the second subtractor input (delay element 56 output connected to subtractor 68 input in figure 2); and

Wherein the subtractor output is connected to the differentiator output (subtractor 76 output connected to differentiator circuit output in figure 2).

11. **As to claim 29,** the claim is rejected for the same reasons as claim 1 above.

12. **As to claim 30,** the claim is rejected for the same reasons as claim 15 above.

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 2-14 and 16-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over McCaslin in view of Applicant admitted prior art (hereafter AAPA).

15. **As to claim 2,** McCaslin does not disclose a multi-channel numerically controlled oscillator comprising the integrator of claim 1.

However, AAPA discloses a multi-channel numerically controlled oscillator comprising the integrator of claim 1 (Page 5, lines 11-28, disclose a standard multi-channel numerically controlled oscillator).

16. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of McCaslin, by incorporating a numerically controlled oscillator with integrators and differentiators, as taught by AAPA for the benefit of generating sinusoidal signals of desired frequencies for various functions in programmable devices (AAPA page 5, lines 12-13). One would be motivated to make the combination, as an NCO is a standard known device to one of ordinary skill in the art to be used to generate a desired frequency.

17. **As to claim 3,** AAPA discloses phase incrementer input multiplexer connected to the integrator input (phase incrementer inputs 302a-302N in figure 3B); and

A sine/cosine generation unit connected to the integrator output (sine/cosine generator in figure 3B).

18. **As to claims 4, 5, 8, 9 and 12,** AAPA discloses the numerically controlled oscillator is an M channel numerically controlled oscillator (inputs from 302a-302N thus having M channels) and McCaslin further discloses the delay section of the integrator comprises at least M delay elements in series (M delay elements such as delay elements 38, 40, and 42 in figure 2).

19. **As to claim 6,** AAPA discloses a down sampler having a down-sampler input connected to the integrator output and a down-sampler output; and a differentiator connected to the down-sampler output (decimator of Figure 1A).

20. **As to claims 7 and 11,** McCaslin further discloses at least N instances of integrator of claim 1 in series (Integrators 38, 40, and 42 in series).

21. **As to claim 10,** AAPA discloses an up-sampler having an up-sampler output connected to the integrator input and an up-sampler input; and a differentiator connected to the up-sampler input (interpolator of Figure 1B).

22. **As to claim 13,** McCaslin further discloses the integrator is implemented in a programmable device (column 5, lines 52-57).

23. **As to claim 14,** McCaslin further discloses the delay section is implemented in one or more embedded memory blocks in a programmable device (Inherent in the delay elements of figure 2, as they need to be embedded in memory in order to operate.).

24. **As to claims 16, 19, 20 and 23,** the claims are rejected for the same reasons as claim 5, 8, 9, and 12 above as applied to the differentiator circuit 16 of figure 2 containing M delay elements such as delay elements 70, 72, and 76.

25. **As to claim 17,** the claim is rejected for the same reasons as claim 6 above.

26. **As to claims 18 and 22,** McCaslin further discloses at least N instances of the differentiator of claim 15 in series (differentiators 56, 58, and 60 in series).

27. **As to claim 21,** the claim is rejected for the same reasons as claim 10 above.

28. **As to claims 24 and 25,** the claims are rejected for the same reasons as claims 13 and 14 above.

29. **As to claim 26,** the claim is rejected for the same reasons as claims 1 and 15 above, in addition, McCaslin discloses N integrators connected in series between the integrator section input and the integrator section output (integrators 38, 40, and 42 in figure 2).

30. McCaslin does not disclose the integrator section comprising a multiplexer comprising M multiplexer inputs and a multiplexer output.

However, McCaslin discloses the integrator section comprising a multiplexer comprising M multiplexer inputs and a multiplexer output (Figure 2 and column 5, lines 15-20 disclose a multiplexer circuit 18 connected to the differentiator output. However, it would have been obvious to one of ordinary skill in the art to place a multiplexer, in

similar fashion to multiplexer 18, connected to the integrator input as multiplexing many channels and signals is well known to one of ordinary skill in the art.).

31. McCaslin does not disclose a down-sampler comprising a down-sampler input connected to the integrator section output and a down-sampler output connected to the differentiator section input.

However, AAPA discloses a down-sampler comprising a down-sampler input connected to the integrator section output and a down-sampler output connected to the differentiator section input (figure 1A).

32. Therefore, it would have been obvious to one of ordinary skill in the art to modify the teachings of McCaslin, by utilizing a decimator providing down-sampling as taught by AAPA, as decimators are frequently used in digital modulation and demodulation circuits and proper conditioning of a signal is critical to proper digital signal processing (page 3, lines 7-13).

33. **As to claim 27,** the claim is rejected for the same reasons as claims 1 and 15 above; in addition, McCaslin does not disclose the differentiator section input comprising a multiplexer comprising M multiplexer inputs and a multiplexer output.

However, McCaslin discloses the differentiator section input comprising a multiplexer comprising M multiplexer inputs and a multiplexer output (Figure 2 and column 5, lines 15-20 disclose a multiplexer circuit 18 connected to the differentiator

output. However, it would have been obvious to one of ordinary skill in the art to place a multiplexer, in similar fashion to multiplexer 18, connected to the differentiator input as multiplexing many channels and signals is well known to one of ordinary skill in the art.).

34. McCaslin does not disclose an up-sampler comprising an up-sampler input connected to the differentiator section output and an up-sampler output connected to the integrator section input.

However, AAPA discloses an up-sampler comprising an up-sampler input connected to the differentiator section output and an up-sampler output connected to the integrator section input (figure 1B).

35. Therefore, it would have been obvious to one of ordinary skill in the art to modify the teachings of McCaslin, by utilizing an interpolator providing up-sampling as taught by AAPA, as interpolators are frequently used in digital modulation and demodulation circuits and proper conditioning of a signal is critical to proper digital signal processing (page 3, lines 7-13).

36. **As to claim 28,** the claim is rejected for the same reasons as claim 1 above; and in addition McCaslin does not disclose an oscillator input comprising M multiplexer inputs and a multiplexer output.

However, McCaslin discloses utilizing a multiplexer at the differentiator output (Figure 2 and column 5, lines 15-20 disclose a multiplexer circuit 18), thus making it

obvious to one of ordinary skill in the art to place a multiplexer connected to an oscillator input as multiplexing many channels and signals is well known to one of ordinary skill in the art.).

37. McCaslin does not disclose a sine/cosine generator having a generator input. However, AAPA discloses a sine/cosine generator having a generator input (figure 3B).

38. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of McCaslin, by implementing a numerically controlled oscillator having a sine/cosine generator, as taught by AAPA, in order to generate sinusoidal signals of desired frequencies for various functions in programmable devices (AAPA page 5, lines 12-13). One would be motivated to make the combination, as an NCO is a standard known device to one of ordinary skill in the art to be used to generate a desired frequency.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Yaary whose telephone number is (571) 270-1249. The examiner can normally be reached on Monday-Friday, 8:00 a.m - 5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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